**Unit III**

**PART-A**

| **Q.No** | **Question** |  |  |
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| 1. | The general purpose registers are combined into a block called as \_\_\_\_\_\_. **a) Register bank**  b) Register Case  c) Register file  d) None of the above |  |  |
| 2. | In \_\_\_\_\_\_ technology, the implementation of the register file is by using an array of memory locations. **a) VLSI**  b) ANSI  c) ISA  d) ASCI |  |  |
| 3. | In a three BUS architecture, how many input and output ports are there ? a) 2 output and 2 input  **b) 1 output and 2 input**  c) 2 output and 1 input  d) 1 output and 1 input |  |  |
| 4. | The main advantage of multiple bus organization over single bus is, a) Reduction in the number of cycles for execution  b) Increase in size of the registers  **c) Better Connectivity**  d) None of these |  |  |
| 5. | CISC stands for, a) Complete Instruction Sequential Compilation  b) Computer Integrated Sequential Compiler  **c) Complex Instruction Set Computer**  d) Complex Instruction Sequential Compilation |  |  |
| 6. | . If the instruction Add R1,R2,R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation) a) 3  **b) ~2**  c) ~1  d) 6 |  |  |
| 7. | In multiple BUS organisation \_\_\_\_\_\_\_\_\_\_ is used to select any of the BUSes for input into ALU. **a) MUX**  b) DE-MUX  c) En-CDS  d) None of the above |  |  |
| 8. | \_\_\_\_\_\_\_\_ are the different type/s of generating control signals. a) Micro-programmed  b) Hardwired  c) Micro-instruction  **d) Both a and b** |  |  |
| 9. | The type of control signal are generated based on, a) contents of the step counter  b) Contents of IR  c) Contents of condition flags  d) All of the above |  |  |
| 10. | What does the hardwired control generator consist of ? a) Decoder/encoder  b) Condition codes  c) Control step counter  d) All of the above |  |  |
| 11. | What does the end instruction do ? **a) It ends the generation of a signal**  b) It ends the complete generation process  c) It starts a new instruction fetch cycle and resets the counter  d) It is used to shift the control to the processor |  |  |
| 12. | What does the RUN signal do ? a) It causes the termination of a signal  b) It causes a particular signal to perform its operation  **c) It causes a particular signal to end** d) It increments the step counter by one |  |  |
| 13. | The benefit of using hardwired approach is a) It is cost effective  b) It is highly efficient  **c) It is very reliable**  d) It increases the speed of operation |  |  |
| 14. | The disadvantage/s of the hardwired approach is a) It is less flexible  b) It cannot be used for complex instructions  **c) It is costly**  d) Both a and b |  |  |
| 15. | In micro-programmed approach, the signals are generated by \_\_\_\_\_\_. **a) Machine instructions**  b) System programs  c) Utility tools  d) None of the above |  |  |
| 16. | A word whose individual bits represent a control signal is \_\_\_\_\_\_. a) Command word  **b) Control word**  c) Co-ordination word  d) Generation word |  |  |
| 17. | A sequence of control words corresponding to a control sequence is called \_\_\_\_\_\_\_. **a) Micro** **routine**  b) Micro function  c) Micro procedure  d) None of the above |  |  |
| 18. | . Individual control words of the micro routine are called as \_\_\_\_\_\_. a) Micro task  b) Micro operation  **c) Micro instruction**  d) Micro command |  |  |
| 19. | The special memory used to store the micro routines of a computer is \_\_\_\_\_\_\_\_. a) Control table  **b) Control store**  c) Control mart  d) Control shop |  |  |
| 20. | To read the control words sequentially \_\_\_\_\_\_\_\_\_ is used. a) PC  **b) IR**  c) UPC  d) None of the above |  |  |

**PART-B**

| **Q.No** | **Question** | **Text book** | **Blooms Taxonomy Level** |
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| 21. | \_\_\_\_\_\_ have been developed specifically for pipelined systems. a) Utility software  **b) Speed up utilities**  c) Optimizing compilers  d) None of the mentioned |  |  |
| 22. | The pipelining process is also called as \_\_\_\_\_\_. a) Superscalar operation  b) Assembly line operation  **c) Von neumann cycle**  d) None of the mentioned |  |  |
| 23. | The fetch and execution cycles are interleaved with the help of \_\_\_\_\_\_\_\_. a) Modification in processor architecture  **b) Clock**  c) Special unit  d) Control unit |  |  |
| 24. | Each stage in pipelining should be completed within \_\_\_\_ cycle. a) 1  b) 2  c) 3  **d) 4** |  |  |
| 25. | If a unit completes its task before the allotted time period, then a) It’ll perform some other task in the remaining time  b) Its time gets reallocated to different task **c) It’ll remain idle for the remaining time**  d) None of the mentioned |  |  |
| 26. | To increase the speed of memory access in pipelining, we make use of \_\_\_\_\_\_\_. a) Special memory locations  **b) Special purpose registers**  c) Cache  d) Buffers |  |  |
| 27. | The periods of time when the unit is idle is called as \_\_\_\_\_. a) Stalls  b) Bubbles  c) Hazards  **d) Both a and b** |  |  |
| 28. | The contention for the usage of a hardware device is called as \_\_\_\_\_\_. **a) Structural hazard**  b) Stalk  c) Deadlock  d) None of the mentioned |  |  |
| 29. | Any condition that causes a processor to stall is called as \_\_\_\_\_. **a) Hazard**  b) Page fault  c) System error  d) None of the above |  |  |
| 30. | The periods of time when the unit is idle is called as \_\_\_\_\_. **a) Stalls**  b) Bubbles  c) Hazards  **d) Both a and b** |  |  |

**PART-C**

| **Q.No** | **Question** | **Text book** | **Blooms Taxonomy Level** |
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| 31. | **Various Hazards**  i) The contention for the usage of a hardware device is called as \_\_\_\_\_\_. **a) Structural hazard**  b) Stalk  c) Deadlock  d) None of the above  ii) The situation where in the data of operands are not available is called \_\_\_\_\_\_. **a) Data hazard**  b) Stock  c) Deadlock  d) Structural hazard  iii) The stalling of the processor due to the unavailability of the instructions is called as \_\_\_\_. **a) Control hazard**  b) Structural hazard  c) Input hazard  d) None of the above  iv) The time lost due to branch instruction is often referred to as \_\_\_\_\_. a) Latency b) Delay  **c) Branch penalty**  d) None of the above |  |  |
| 32. | Algorithm used in Concurrency:  i) The algorithm followed in most of the systems to perform out of order execution is \_\_\_\_\_\_. **a) Tomasulo algorithm**  b) Score carding  c) Reader-writer algorithm  d) None of the above  ii). The problem where process concurrency becomes an issue is called as \_\_\_\_\_\_. a) Philosophers problem  b) Bakery problem  **c) Bankers problem**  d) Reader-writer problem |  |  |
| 33. | Bus Structure:  i) Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus? (A) 1 Megabyte/sec  (B) 4 Megabytes/sec  (C) 8 Megabytes/sec  **(D) 2 Megabytes/sec**  **ii)** The communication between the components in a microcomputer takes place via the address and  (A) I/O bus  **(B) Data bus**  (C) Address bus  (D) Control lines |  |  |
| 34. | **Micro Programmed Control**  **i)** A microprogram sequencer  **(A) generates the address of next micro instruction to be executed.**  (B) generates the control signals to execute a microinstruction.  (C) sequentially averages all microinstructions in the control memory.  (D) enables the efficient handling of a micro program subroutine.  ii) The operation executed on data stored in registers is called  (A) Macro-operation  **(B) Micro-operation**  (C) Bit-operation  (D) Byte-operation |  |  |
| 35. | Hard Wired Control  i) Hardwired control unit uses \_\_\_\_to interpret an instruction  **a) Special Program**  b) Special micro  c) fixed logic  d) instruction register  ii) While designing hardwired control unit factor to be considered  a) amount of hardware used  b) Speed of operation  c) cost of design  **d) all of the above** |  |  |